PIC16(L)F1777/8/9

PIC16(L)F1777/8/9 Family
Silicon Errata and Data Sheet Clarification

The PIC16(L)F1777/8/9 family devices that you have received conform functionally to the current Device Data Sheet (DS40001819**B**), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in Table 1. The silicon issues are summarized in Table 2.

The errata described in this document will be addressed in future revisions of the PIC16(L)F1777/8/9 silicon.

Note:	This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated in the last column of Table 2 apply to the current silicon revision (**A1**).

Data Sheet clarifications and corrections start on page 5, following the discussion of silicon issues.

The silicon revision level can be identified using the current version of MPLAB® IDE and Microchip's programmers, debuggers, and emulation tools, which are available at the Microchip corporate website (www.microchip.com).

For example, to identify the silicon revision level using MPLAB IDE in conjunction with a hardware debugger:

1. Using the appropriate interface, connect the device to the hardware debugger.
2. Open an MPLAB IDE project.
3. Configure the MPLAB IDE project for the appropriate device and hardware debugger.
4. Based on the version of MPLAB IDE you are using, do one of the following:
   a) For MPLAB IDE 8, select *Programmer > Reconnect*.
   b) For MPLAB X IDE, select *Window > Dashboard* and click the **Refresh Debug Tool Status** icon ( ).
5. Depending on the development tool used, the part number *and* Device Revision ID value appear in the **Output** window.

Note:	If you are unable to extract the silicon revision level, please contact your local Microchip sales office for assistance.

The DEVREV values for the various PIC16(L)F1777/8/9 silicon revisions are shown in Table 1.

TABLE 1: SILICON DEVREV VALUES

Part Number	Device ID(1)	Revision ID Silicon Revision(2)	
		A0	A1
PIC16F1777	308Eh	2000h	2001h
PIC16LF1777	3091h	2000h	2001h
PIC16F1778	308Fh	2000h	2001h
PIC16LF1778	3092h	2000h	2001h
PIC16F1779	3090h	2000h	2001h
PIC16LF1779	3093h	2000h	2001h

Note 1: The Device ID is located in the configuration memory at address 8006h.

2: Refer to the *"PIC16(L)F177X Memory Programming Specification"* (DS40001792) for detailed information on Device and Revision IDs for your specific device.

TABLE 2: SILICON ISSUE SUMMARY

Module	Feature	Item Number	Issue Summary	Affected Revisions[1]	
				A0	A1
Enhanced Universal Synchronous Receiver Transmitter (EUSART)	Transmit mode	1.1	Possible duplicate byte transmitted.	X	
Master Synchronous Serial Port (MSSP)	SPI Slave mode	2.1	SPI master releasing Slave Select during Slave Sleep mode corrupts data.	X	
Master Synchronous Serial Port (MSSP)	SPI Slave mode	2.2	SPI master enabling Slave Select too early could lose received data in Slave mode.	X	
Master Synchronous Serial Port (MSSP)	SPI Slave mode	2.3	WCOL is erroneously set in SPI Slave mode during Sleep.	X	
Programmable Ramp Generator (PRG)	Timing Sources	3.1	Configurable Logic Cell (CLC) timing sources not available.	X	
Programmable Ramp Generator (PRG)	Ramp Capacitor	3.2	Ramp capacitor shorting switch fails to stay closed.	X	X
ECCP	Compare mode	4.1	Compare Toggle mode yields unexpected results.	X	X

Note 1: Only those issues indicated in the last column apply to the current silicon revision.

Silicon Errata Issues

Note: This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated by the shaded column in the following tables apply to the current silicon revision (**A1**).

1. Module: Enhanced Universal Synchronous Receiver Transmitter (EUSART)

1.1 Transmit Mode

Under certain conditions, a byte written to the TXxREG register can be transmitted twice. This happens when a byte is written to TXxREG just as the TSR register becomes empty. This new byte is immediately transferred to the TSR register, but also remains in the TXxREG register until the completion of the current instruction cycle. If the new byte in the TSR register is transmitted before this instruction cycle has completed, the duplicate in the TXxREG register will subsequently be transferred to the TSR register on the following instruction clock cycle and transmitted.

Work around

When transmitting bytes, it is common practice to check the TXIF bit before writing to the TXxREG register. To avoid the issue of duplicate bytes being transmitted, a NOP should be placed before the write to the TXxREG register. This changes the timing so that the issue does not occur. The TRMT bit can also be checked in addition to or instead of the TXIF bit to determine if TXxREG can be written without causing a duplicate byte transmission. If the Transmit Interrupt is enabled, then inside the Interrupt Service Routine (ISR) testing, the TRMT bit will avoid transmission of a duplicate byte.

Affected Silicon Revisions

A0	A1						
X							

2. Module: Master Synchronous Serial Port (MSSP)

2.1 SPI Slave Mode

When the MSSP module is configured in SPI Slave mode with $\overline{SS}$ pin control enabled (SSPM = 0100) and the device is in Sleep mode during SPI activity, if the SPI master releases the $\overline{SS}$ line ($\overline{SS}$ goes high) before the device wakes from Sleep and updates SSPxBUF, the received data will be lost.

Work around

Method 1: The SPI master must wait a minimum of parameter SP83 (1.5 T_{CY} + 40 ns) after the last SCK edge and the additional wake-up time from Sleep (device dependent) before releasing the $\overline{SS}$ line.

Method 2: If both the master and slave devices have an available pin, once the slave has completed the transaction and BF or SSPIF is set, the slave could toggle an output to inform the master that the transaction is complete and that it is safe to release the $\overline{SS}$ line.

Affected Silicon Revisions

A0	A1						
X							

2.2 SPI Slave Mode

When the MSSP module is configured in SPI Slave mode with $\overline{SS}$ pin control enabled (SSPM = 0100) and the device is in Sleep mode during SPI activity, if the SPI master enables $\overline{SS}$ ($\overline{SS}$ goes low) within 1 T_{CY} before Sleep is executed, the data written into the SSPxBUF by the slave for transmission will remain in the SSPxBUF, and the byte received by the slave will be completely discarded. The MSb of the data byte that is currently loaded into SSPxBUF will be transmitted on each of the eight SCK clocks, resulting in either a 0x00 or 0xFF to be incorrectly transmitted. This issue typically occurs when the device wakes up from Sleep to process data and immediately goes back to Sleep during the next transmission.

Work around

The SPI slave must wait a minimum of 2.25 * T_{CY} from the time the $\overline{SS}$ line becomes active ($\overline{SS}$ goes low) before executing the Sleep command.

Affected Silicon Revisions

A0	A1						
X							

2.3 SPI Slave Mode

When the MSSP module is configured with either of the Slave modes listed below and Sleep is executed during transmission, the WCOL bit is erroneously set. Although the WCOL bit is set, it does not cause a break in transmission or reception.

Mode 1: SPI Slave mode with $\overline{SS}$ disabled (SSPM = 0101) and CKE = 0.

Mode 2: SPI Slave mode with $\overline{SS}$ enabled (SSPM = 0100) and $\overline{SS}$ not set and then cleared before each consecutive transmission. This typically occurs during multiple byte transmissions in which the master does not release the $\overline{SS}$ line until all transmission has completed.

Work around

Method 1: The WCOL bit can be ignored since the issue does not interfere with MSSP hardware.

Method 2: Clear the SSPEN bit after each transaction, then set SSPEN before next transaction.

Affected Silicon Revisions

A0	A1						
X							

3. Module: Programmable Ramp Generator (PRG)

3.1 Timing Sources

The Configurable Logic Cell (CLC) timing sources LC1_out, LC2_out, LC3_out, and LC4_out as defined in Table 30-5 of the data sheet are not available in the A0 revision. Use of these resources will result in unexpected operation.

Work around

None.

Affected Silicon Revisions

A0	A1						
X							

3.2 Ramp Capacitor Shorting Switch Fails to Stay Closed

When the PRG GO bit is zero or when the rising or falling ramp is in the Reset state for an extended period of time, then the ramp capacitor shorting switch will improperly open, causing the PRG output to drift from the reference voltage input level.

Work around

None.

Affected Silicon Revisions

A0	A1						
X	X						

4. Module: ECCP

4.1 Compare Mode

The ECCP Compare Toggle mode (CCP1M<3:0> bits = 0010) works properly as long as the Timer1 Prescaler value is configured to 1:1. When the Timer1 prescaler value is configured to any other value, the ECCP compare output yields unexpected results.

Work around

Only use the Compare Toggle mode when the Timer1 Prescaler value is set to 1:1.

Affected Silicon Revisions

A0	A1						
X	X						

Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (DS40001819**B**):

Note:	Corrections are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

None.

APPENDIX A: DOCUMENT REVISION HISTORY

Rev A Document (12/2015)

Initial release of this document.

Rev B Document (12/2017)

Added Revision A1 in Table 1 and Table 2; Table 2: added Ramp Capacitor; Module 3: Added 3,2.

DS Clarifications: removed Module Bank 6 and Table 3-4, Table 3-18, Module Bank 12, Table 3-6 and Table 3-7.

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ISBN: 978-1-5224-2500-7

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